WHAT IS CLAIMED IS:

1. An apparatus including a fade controller for providing programmable fade rates for an on-screen display (OSD) window within a video display, comprising:

accumulation circuitry that responds to reception of a plurality of accumulation control signals and respective programmable vertical and horizontal fade interval data signals corresponding to respective programmable vertical and horizontal OSD fade intervals by providing respective pluralities of cumulative vertical and horizontal fade interval data signals corresponding to respective pluralities of cumulative vertical and horizontal OSD fade intervals;

counting circuitry, coupled to said accumulation circuitry, that responds to reception of a plurality of timing control signals and said pluralities of cumulative vertical and horizontal fade interval data signals by providing vertical and horizontal count signals corresponding to respective completions of said cumulative vertical and horizontal OSD fade intervals; and

encoding circuitry, coupled to said counting circuitry, that responds to reception of a plurality of OSD window control signals and said vertical and horizontal count signals by providing an OSD fade control signal corresponding to occurrence of said OSD window within said video display.

2. The apparatus of claim 1, wherein:

said fade controller is for providing programmable fade in and fade out rates for said OSD window within said video display;

for vertical fading of said OSD window,

said programmable vertical OSD fade interval is shorter than each one of said plurality of cumulative vertical OSD fade intervals during fade in, and

said programmable vertical OSD fade interval is longer than each one of said plurality of cumulative vertical OSD fade intervals during fade out; and

for horizontal fading of said OSD window,

said programmable horizontal OSD fade interval is shorter than each one of said plurality of cumulative horizontal OSD fade intervals during fade in, and

said programmable horizontal OSD fade interval is longer than each one of said plurality of cumulative horizontal OSD fade intervals during fade out.

3. The apparatus of claim 1, wherein said accumulation circuitry comprises:

adder circuitry that responds to reception of at least a first one of said plurality of accumulation control signals, said programmable vertical and horizontal fade interval data signals, and said pluralities of cumulative vertical and horizontal fade interval data signals by adding said programmable vertical and horizontal fade interval data signals with corresponding ones of said pluralities of cumulative vertical and horizontal fade interval data signals to provide next ones of said pluralities of cumulative vertical and horizontal fade interval data signals;

multiplexor circuitry, coupled to said adder circuitry, that responds to reception of at least a second one of said plurality of accumulation control signals, said programmable vertical and horizontal fade interval data signals, and said next ones of said pluralities of cumulative vertical and horizontal fade interval data signals by selecting between said programmable vertical and horizontal fade interval data signals and said next ones of said pluralities of cumulative vertical and horizontal fade interval data signals to provide selected vertical and horizontal fade interval data signals; and

register circuitry, coupled to said multiplexor circuitry and said adder circuitry, that responds to reception of at least a third one of said plurality of accumulation control signals and said selected vertical and horizontal fade interval data signals by storing said selected vertical and horizontal fade interval data signals to be provided as said pluralities of cumulative vertical and horizontal fade interval data signals.

4. The apparatus of claim 1, wherein said plurality of accumulation control signals comprises:

at least one fade in/out control signal determinative of whether each one of said plurality of cumulative vertical OSD fade intervals is longer or shorter than said programmable vertical OSD fade interval and whether each one of said plurality of cumulative horizontal OSD fade intervals is longer or shorter than said programmable horizontal OSD fade interval;

at least one data selection control signal determinative of when one of said plurality of cumulative vertical OSD fade intervals is equal to said programmable vertical OSD fade interval and when one of said plurality of cumulative horizontal OSD fade intervals is equal to said programmable horizontal OSD fade interval; and

at least one interval timing control signal determinative of when successive ones of said plurality of cumulative vertical OSD fade intervals increase or decrease in duration and when successive ones of said plurality of cumulative horizontal OSD fade intervals increase or decrease in duration.

5. The apparatus of claim 1, wherein said counting circuitry comprises:

a first counter that responds to reception of a first portion of said plurality of timing control signals by loading and counting from said plurality of cumulative vertical fade interval data signals to provide said vertical count signals; and

a second counter that responds to reception of a second portion of said plurality of timing control signals by loading and counting from said plurality of cumulative horizontal fade interval data signals and to provide said horizontal count signals.

6. The apparatus of claim 1, wherein said plurality of timing control signals comprises:

at least one interval timing control signal determinative of when successive ones of said plurality of cumulative vertical fade interval data signals are used in initiating a vertical count sequence to produce said vertical count signal and when successive ones of said plurality of cumulative horizontal fade interval data signals are used in initiating a horizontal count sequence to produce said horizontal count signal; and

at least one count control signal determinative of vertical and horizontal count rates for said vertical and horizontal count sequences, respectively.

7. The apparatus of claim 1, wherein said encoding circuitry comprises:

register circuitry that responds to reception of a portion of said plurality of OSD window control signals by storing said vertical and horizontal count signals; and

logic circuitry, coupled to said register circuitry, that logically combines another portion of said plurality of OSD window control signals and said stored vertical and horizontal count signals to provide said OSD fade control signal.

8. The apparatus of claim 1, wherein said plurality of OSD window control signals comprises:

at least one timing control signal determinative of when said vertical and horizontal count signals are encoded with said plurality of OSD window control signals; and

at least one OSD enablement signal determinative of when said OSD fade control signal is active.

9. The apparatus of claim 1, further comprising sequencer circuitry, coupled to said accumulation circuitry, said counting circuitry and said encoding circuitry, that responds to reception of a plurality of control signals for said video display by providing said plurality of accumulation control signals, said plurality of timing control signals and said plurality of OSD window control signals.

10. The apparatus of claim 9, wherein said sequencer circuitry comprises:

vertical state machine circuitry, coupled to first respective portions of said accumulation circuitry, said counting circuitry and said encoding circuitry, that responds to reception of a first portion of said plurality of control signals for said video display by providing first respective portions of said plurality of accumulation control signals, said plurality of timing control signals and said plurality of OSD window control signals; and

horizontal state machine circuitry, coupled to second respective portions of said accumulation circuitry, said counting circuitry and said encoding circuitry, that responds to reception of a second portion of said plurality of control signals for said video display by providing second respective portions of said plurality of accumulation control signals, said plurality of timing control signals and said plurality of OSD window control signals.

11. An apparatus including a fade controller for providing programmable fade rates for an on-screen display (OSD) window within a video display, comprising:

accumulator means for receiving a plurality of accumulation control signals and respective programmable vertical and horizontal fade interval data signals corresponding to respective programmable vertical and horizontal OSD fade intervals and in response thereto generating respective pluralities of cumulative vertical and horizontal fade interval data signals corresponding to respective pluralities of cumulative vertical and horizontal OSD fade intervals;

counter means for receiving a plurality of timing control signals and said pluralities of cumulative vertical and horizontal fade interval data signals and in response thereto generating vertical and horizontal count signals corresponding to respective completions of said cumulative vertical and horizontal OSD fade intervals; and

encoder means for receiving a plurality of OSD window control signals and said vertical and horizontal count signals and in response thereto generating an OSD fade control signal corresponding to occurrence of said OSD window within said video display.

12. The apparatus of claim 11, further comprising sequencer means for receiving a plurality of control signals for said video display and in response thereto generating said plurality of accumulation control signals, said plurality of timing control signals and said plurality of OSD window control signals.

13. A method of fade control for applying programmable fade rates to an on-screen display (OSD) window within a video display, comprising:

vertically fading said OSD window using a programmable vertical OSD interval value corresponding to a vertical dimension of said OSD window; and

horizontally fading said OSD window using a programmable horizontal OSD interval value corresponding to a horizontal dimension of said OSD window;

with each of said fadings performed by

providing said programmable OSD interval value;

storing said programmable OSD interval value;

enabling said OSD window;

counting during a time interval corresponding to said stored OSD interval value;

disabling said OSD window following termination of said time interval count;

combining said programmable and stored OSD interval values to provide a cumulative OSD interval value;

substituting said cumulative OSD interval value for said stored OSD interval value;

repeating said enabling, counting, disabling, combining and substituting until a predetermined cumulative OSD interval value has been reached.

14. The method of claim 13, wherein said counting during a time interval corresponding to said stored OSD interval value comprises counting down from said stored OSD interval value.

15. The method of claim 13, wherein said counting during a time interval corresponding to said stored OSD interval value comprises counting up from said stored OSD interval value.

16. The method of claim 13, wherein said combining said programmable and stored OSD interval values to provide a cumulative OSD interval value comprises adding said programmable and stored OSD interval values to provide a higher cumulative OSD interval value.

17. The method of claim 13, wherein said combining said programmable and stored OSD interval values to provide a cumulative OSD interval value comprises computing a difference between said programmable and stored OSD interval values to provide a lower cumulative OSD interval value.

18. The method of claim 13, wherein said substituting said cumulative OSD interval value for said stored OSD interval value comprises selecting said cumulative OSD interval value in place of said programmable OSD interval value.